phase difference value into reference values corresponding to phase differences generated when FFT window errors of at least one sample exist, thereby to generate a normalized value; and

(c) simultaneously controlling the FFT window position offset using a value obtained by rounding off the normalized value of the step (b), and the sampling clock offset using the difference between the round-off value and the normalized value.

3. (Amended) An OFDM receiver for interlocking FFT window position recovery with sampling clock control by receiving an OFDM symbol consisting of a useful data interval and a guard interval, the apparatus comprising:

an analog-to-digital converter (ADC) for converting an OFDM signal into digital complex samples;

an FFT window for removing the guard interval from the digital complex samples output by the ADC and outputting useful data samples;

an FFT for fast-Fourier-transforming the samples output by the FFT window;

a phase difference calculator for calculating phase differences between two values among the complex values received via a plurality of pilots from the FFT, averaging [these] the phase differences for one symbol to generate a mean phase difference value, and normalizing the mean phase difference value by dividing [it] the mean phase difference value into predetermined reference values;

an FFT window controller for rounding off the normalized value output by the phase difference calculator and controlling the window position of the FFT window; and

a phase synchronous loop for controlling the sampling clock signals of the ADC using the difference between the round-off value and the normalized value.

4. (Amended) The OFDM receiver for interlocking FFT window position recovery with sampling clock control as claimed in claim 3, wherein the phase difference calculator comprises:

a phase difference detector for detecting the phase differences between two pilots among the received complex values of the pilots output by the FFT;